Smart camera design for realtime High Dynamic Range imaging

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High dynamic range smart camera

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Many camera sensors suffer from limited dynamic range. The result is that there is a lack of clear details in displayed images and videos.

This presentation describes our approach to generate high dynamic range (HDR) from an image sequence while modifying exposure times for each new frame. For this purpose, we propose an FPGA-based architecture that can produce a real-time high dynamic range video from successive image acquisition. Our hardware platform is built around a standard low dynamic range (LDR) CMOS sensor and a Virtex 5 FPGA board. The CMOS sensor is a EV76C560 provided by e2v. This 1.3 Megapixel device offers novel pixel integration/readout modes and embedded image pre-processing capabilities including multiframe acquisition with various exposure times.

Our approach consists of hardware architecture with different algorithms: double exposure control during image capture, building of an HDR image by combining the multiple frames, and final tone mapping for viewing on a LCD display.

Our stationary video camera system is able to achieve a real-time video rate of 30 frames per second for a full sensor resolution of 1280x1024 pixels.